

How fast are semiconductor prices falling?*

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Abstract

The Producer Price Index (PPI) for the United States suggests that semiconductor prices have barely been falling in recent years, a dramatic contrast from the rapid declines reported from the mid-1980s to the early 2000s. This slowdown in the rate of decline is puzzling in light of evidence that the performance of microprocessor units (MPUs) has continued to improve at a rapid pace. Roughly coincident with the shift to slower price declines in the PPI, Intel — the leading producer of MPUs — substantially changed its pricing behavior and model introduction strategy for these chips. We argue that, with the changes in Intel's pricing behavior, the matched-model methodology used in the PPI for MPUs likely started to be biased in the mid-2000s and that hedonic indexes provide a more accurate measure of price change since then. Our preferred hedonic index of MPU prices tracks the PPI closely through 2008. However, from 2008 to 2012, our preferred index fell at an average annual rate of 39 percent, while the PPI declined at only a 9 percent rate. Given that MPUs represent about half of U.S. shipments of semiconductors, this difference has important implications for gauging the rate of innovation in the semiconductor sector.

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1. Introduction

How fast are semiconductor prices falling? Data from the Producer Price Index (PPI) for the United States suggest that prices of microprocessor units (MPUs) have barely been falling in recent years. This very slow rate of price decline stands in sharp contrast to the rapid declines in MPU prices reported from the mid-1980s up to the early 2000s and the exceptionally rapid declines in the latter half of the 1990s. If correct, the apparent slowdown in MPU price declines in recent years would be troubling, given the long-run relationship between rates of price decline for semiconductors and the pace of innovation in that sector.¹

A stalling out of innovation in this sector likely would have broader implications for the economy, as semiconductors are an important general-purpose technology lying behind machine learning, robotics, big data, massive connectivity, and many other ongoing advances.² Indeed, adverse developments in the semiconductor sector ultimately would damp the growth potential of the overall economy.³ On the other hand, if technological progress and attendant price declines were to continue at a rapid pace, powerful incentives would be in place for continued development and diffusion of new applications of this general-purpose technology.

The apparent slowdown in the rate of price decline is puzzling given evidence that the performance of MPUs continued to improve at a rapid pace after the mid-2000s. The key to resolving the puzzle may reside in another development in the semiconductor industry. Roughly coincident with the shift to a slower pace of price decline in the PPI, Intel — the leading MPU producer — dramatically changed its pricing and model introduction behavior. Prior to the mid-2000s, Intel generally introduced new chips at the technological cutting edge and lowered the list

¹ See Aizcorbe, Oliner, and Sichel (2008) for a discussion of the relationship between price change and innovation for semiconductors.

² McKinsey (2013) highlights key innovations in many sectors of the economy.

³ For discussions of the sources of a possible slowdown in the underlying pace of economic growth, see Cowen (2011), Fernald (2014), Gordon (2012 and 2013), Hall (2014), and Jorgenson, Ho, and Samuels (2013).

prices of existing chips to remain competitive on a price-performance basis. However, by 2006, Intel had shifted to a new paradigm in which it largely kept the list prices of existing chips unchanged and began introducing new chips both at the frontier and at lower performance levels.

These changes in Intel's behavior could resolve the puzzling disconnect between recent continuing improvements in MPU performance and trends in prices. Namely, we argue that the widely-used matched-model methodology is not well suited to capturing price trends in a regime where producers are setting prices as Intel has since the mid-2000s. In such a pricing regime, if performance is improving over time, then matched-model price indexes—like the PPI for MPUs—likely are biased. We argue that hedonic indexes are better suited to capturing price trends in these circumstances and develop new hedonic indexes for quality-adjusted prices using price data for Intel MPUs from 2000 to 2012. Our preferred index tracks the PPI closely from 2000 to 2008. However, from 2008 to 2012—the period after Intel's new pricing regime was in place—our preferred index of MPU prices fell at an average annual rate of 39 percent, while the PPI declined at only a 9 percent rate.

We focus on MPUs, rather than a broader set of semiconductor products, for several reasons.⁴ First, MPUs are a large segment of the semiconductor sector, representing about half of U.S. shipments (the scope of the PPI). Second, price series for MPUs extend back to the mid-1980s, allowing for comparisons of price trends over time. Given that price trends in this sector often are used to infer rates of technical progress, this historical comparability is important. Finally, we believe that developments in MPU technology likely provide a rough guide to

⁴ Among all MPUs, this paper analyzes prices of the MPUs used in desktop personal computers (PCs), for which data are the most readily available. In other work, we are developing indexes for MPUs going into servers, the types of machines that would support cloud computing in server farms and other processor-intensive applications. In addition, Dan Sichel's undergraduate thesis student, Sophie (Liyang) Sun (2014) developed price indexes for MPUs going into laptop computers.

developments in other parts of the semiconductor sector, such as the chips that are used in smartphones and tablets.⁵

Our work on MPU prices builds on important earlier research. Much prior work on semiconductor prices relied on physical characteristics of the chips to control for quality. Notable studies that have constructed hedonic price indexes for semiconductors with this approach include Cole et al. (1986), Dulberger (1993), Grimm (1998), and Flamm (2007).

Although the physical characteristics used in these studies are correlated with performance, they may not fully capture the capabilities of the processor for end users. For this reason, Triplett (1989) and others called for analysis of MPU prices with controls for more refined measures of performance. In this vein, Chwelos (2000 and 2003) constructed hedonic price indexes for PCs with controls for the results of a suite of benchmark performance tests.⁶

An alternative approach has been to measure semiconductor prices with matched-model indexes. Aizcorbe, Corrado, and Doms (2003) found that under certain circumstances (highly granular data on model prices and high-frequency observations), a matched-model index may produce similar results to a hedonic index. Such highly granular data were used by the Federal Reserve Board in the construction of its MPU price index through 2006, after which point the underlying data were no longer available.

We extend the existing literature in two ways. First, we develop hedonic price indexes for MPUs that control for quality with performance measures based on actual programs

⁵ The market for chips going into smartphones and tablets is changing rapidly, and it is challenging to obtain consistent time series on prices and performance. That being said, the production processes and technologies are similar enough to those for MPUs that developments in MPUs likely provide at least a rough gauge of developments in these other types of chips.

⁶ Grimm (1998) developed specifications that controlled for millions of instructions per second (MIPS), a measure of performance which has limited ability to account for differences across MPUs in the translation of instructions into program execution. In addition, Holdway (2001) examined unit value MPU price indexes using benchmark test scores as a measure of quality-adjusted units of computing power.

representing typical workloads. Second, we use these hedonic price indexes to assess the possibility that the PPI has been understating the price declines for MPUs.

The next section highlights the puzzle raised by the very slow rate of decline in the PPI during recent years at the same time that the engineering frontier for MPUs continued to move out rapidly. Section 3 presents our argument that hedonic price indexes are likely to better capture price trends than are matched-model indexes (such as the PPI) since the mid-2000s when Intel's pricing behavior changed. Section 4 provides a brief review of our data, which cover the period from 2000 to 2012. In section 5, we describe the hedonic regressions used to obtain measures of quality-adjusted prices. Section 6 presents our results, and section 7 concludes.

2. The Puzzle

As noted, the PPI for MPUs has fallen very slowly in recent years. This section explores the plausibility of this extreme slowdown from a few different perspectives. The first perspective is whether the slowdown meshes with the trends in technological advance for MPU chips. The second perspective focuses on the changes that occurred in Intel's pricing patterns for MPUs, developments that, as we show below, have important implications for price index measurement.

*Technology cycles and chip performance.*⁷ The standard definition of a semiconductor technology cycle is the amount of time required to achieve a 30 percent reduction in the width of the smallest feature on a chip. Because chips are rectangular, a 30 percent reduction in both the horizontal and vertical directions implies about a 50 percent reduction (0.7×0.7) in the area required for the smallest chip component. As documented in Byrne, Oliner, and Sichel (2013),

⁷ The text in this section draws heavily on material in Byrne, Oliner, and Sichel (2013). In addition, table 1 comes directly from that paper.

the semiconductor industry has achieved massive reductions in scaling over time. Indeed, the area occupied by a chip component in 2012 was roughly 200,000 times smaller than in 1969.

There is a broad consensus that the pace of technical advance in the semiconductor industry sped up in the mid-1990s, a development first brought to the attention of economists by Jorgenson (2001). Table 1 reports the average length of the semiconductor technology cycle (as defined above) for various periods. For the industry as a whole, the technology cycle averaged three years until 1993 and then dropped to about two years from 1993 to 2012. Within the later period, the scaling advances were especially rapid from 1993 to 2003 and a bit slower after 2003. Even so, the average cycle since 2003 has remained substantially shorter than the three-year cycle in effect before the 1990s. For Intel's MPU chips, there has been no pullback at all from the two-year cycle. The upshot is that the cycles in semiconductor technology — a key driver of quality improvement in IT products — have remained rapid.⁸

While the pace of miniaturization has been sustained, semiconductor producers have changed the approach used to translate these engineering gains into faster performance. Historically, each new generation of technology in semiconductors has allowed for an increase in the number of basic calculations performed per second for a given chip design. However, as speed continued to increase, dissipating the generated heat became problematic. In response, Intel shifted around 2006 toward raising “clockspeed” more slowly and boosted performance instead by placing multiple copies of the core architecture on each chip — a change enabled by smaller feature size — and by improving the design of those cores (see Shenoy and Daniel, 2006).

⁸ These continuous increases in chip density are the force behind Moore's Law, which states that the number of components on leading-edge chips will double every two years. Moore's original formulation (Moore, 1965) pegged the doubling time at only one year, but in 1975 he revised the period to be two years based on the actual experience to that point (Intel Corporation, 2005). For a discussion of the outlook for Moore's Law, see Bauer, Veira, and Weig (2013).

The effect of this strategy on the rate of increase in performance for end users has been a matter of some debate. Pillai (2013) examines the record and presents evidence that scores for Intel MPUs on benchmark performance tests — based on standard tasks designed to reflect the needs of computer users — rose more slowly from 2001 to 2008 than in the 1990s. Our own extension of his results to more recent data suggests that the rate of performance improvement over 2001-08 persisted through 2012 without any further slowdown.⁹ Over the full period from 2001 to 2012, our results show that the end-user performance of Intel’s MPU chips improved roughly 30 percent per year on average. End users have continued to see substantial gains in performance, just not the extraordinary rate of increase recorded in the 1990s.

Historically, these improvements in the engineering frontier have translated into steep declines in MPU prices. Figure 1 shows the annual price declines back to 1986, splicing together estimates from Grimm (1998) through 1992, the Federal Reserve Board for 1993-97, and the PPI for later years. Over this period, MPU prices fell at an average rate of nearly 30 percent per year, with especially sharp drops in the second half of the 1990s. However, reported price declines have slowed dramatically over the past several years. Indeed, the declines in 2010, 2011, and 2012 were smaller than in any prior year back to 1986, breaking the link with the continued engineering improvements. Perhaps the cost of achieving these engineering advances has accelerated in recent years. If that were the case, we might expect to see a similar price pattern for other types of semiconductor chips. No such pattern, though, is evident for memory chips (DRAMs).¹⁰ As shown in figure 2, DRAM prices have been quite volatile from year to year,

⁹ We used SPEC performance data for this analysis. We accessed the data on December 5, 2012 and used the benchmark suites SPEC® CPU2006 and SPEC® CPU2000.

¹⁰ The most important driver of DRAM performance is the size of the components on the chip, which has continued to shrink rapidly, as discussed above. See Flamm (1993) for a discussion of characteristics of DRAM chips.

with no clear trend toward slower declines. At least for DRAMs, then, the translation of the engineering frontier to prices does not appear to have changed.

All in all, the shift to much slower price declines for microprocessors in the PPI is a puzzle in light of the continued substantial improvements on the engineering front. We next consider the possibility that changes in the properties of Intel's posted prices after 2006 could have distorted the measurement of price trends in the PPI.

Pricing, product introduction, and market position. Between 2003 and 2006, the properties of Intel's posted prices for MPU chips changed dramatically.¹¹ Prior to 2003, the price of a specific Intel MPU model tended to drop fairly rapidly in the year or two following its introduction, especially once a new, higher performance model became available. By 2006, this pattern had completely changed; the posted price of a specific model tended to remain constant, even after a new, higher performance model became available at a similar price.

Figure 3 illustrates this shift in pricing behavior, showing the share of Intel desktop MPU models that experienced a price decline within four quarters of introduction.¹² As can be seen, all of the models introduced from 2000 to 2002 experienced at least one price decline during this initial part of their life cycle. The share of chips with a price decline during this phase of the life cycle then fell sharply, dropping to less than 20 percent for the 2012 cohort.

After 2003, Intel also changed its product introduction strategy, as can be seen in figure 4. The black dots for each quarter show the benchmark performance scores for the previously-introduced desktop MPU chips sold in that quarter (the "incumbents"), while the red bars shows

¹¹ While the BLS does not indicate which companies' prices are included in the PPI for MPUs, it is only reasonable to assume that Intel is included given its dominant market position. Moreover, it appears that BLS has been making at least some use of Intel's posted prices for MPUs (see Holdway, 2001).

¹² The price data in the figure are described in section 4.

the performance scores for newly-introduced chips (the "entrants").¹³ During 2000-03, Intel generally introduced new MPU chips at or beyond the frontier of existing technology. However, Intel then moved to a strategy of introducing new models further down its product line. The introduction of new chips well below the frontier is particularly evident in 2005, 2008, and 2012. Table 2 summarizes the changes in chip introduction over time. During 2000-03, 68 percent of Intel's desktop MPU chips had performance scores that exceeded the existing frontier, but this share fell to about 25 percent during 2004-06 and only rebounded partially after 2006. The table also compares the average performance score for all entering chips to the frontier incumbent chip. During 2000-03, the average performance of entering chips was nearly 5 percent above that for the incumbent at the frontier. However, by 2004-06, the average entrant's score had shifted down to be 3½ percent below the frontier incumbent, and the average gap behind the frontier widened further during 2006-09 and 2009-12.

The years from roughly 2003 to 2006, therefore, appear to have been a time of transition for Intel's MPU strategy. By 2006, the company had moved to a business model that featured more active management of its product offerings below the frontier. In addition, by setting list prices that were relatively stable over a chip's life cycle, Intel may have been attempting to extract more revenue from less price-sensitive buyers while offering discounts on a case-by-case basis.

These shifts took place against the backdrop of a changing competitive environment vis-a-vis AMD, its primary challenger in the MPU market. Figure 5 plots Intel's annual revenue from all products (not only MPUs) as a share of Intel and AMD's combined revenue. Over this

¹³ The figure has separate panels for 2000-06 and 2006-12 because of the shift to a new benchmark performance test in 2006. Some of the MPU chips sold in 2006 were evaluated on the old test and some were evaluated on the new test, which explains the presence of 2006 in both panels. The performance scores are described in detail in section 4.

20-year period, Intel's revenue share ranged from just under 80 percent to slightly above 90 percent. In 2002 and 2003, Intel's share stood at the top of this range but then eroded significantly through 2006. Nosko (2010) also documented this share erosion, noting that from 2002 to 2006, AMD "consistently released products whose price/performance characteristics were similar to or beat Intel's" (p. 8). Documents from legal actions against Intel for alleged antitrust violations (see, for example, *State of New York v. Intel Corporation*, 2009) also provide evidence that Intel was concerned about its losses of market share to AMD during this period.

However, in 2006, Intel began to turn the corner by offering new MPUs that dominated those sold by AMD (see Nosko, 2010, for details) and subsequently pulled ahead of AMD in a decisive way, consistent with the recovery in Intel's overall revenue share. Figure 6 drills down to focus specifically on market shares for MPUs, starting in 2007. From 2007 to 2013, Intel's share of the two manufacturers' combined MPU revenues climbed considerably on net, reflecting sizable gains in each of the product classes plotted in the figure. By 2013, Intel's dominance had reached the point that AMD effectively had been relegated to the bottom end of the MPU market. Indeed, as shown in figure 7, AMD received more than 85 percent of its MPU revenue from chips that sold for less than \$75, the low-end part of the market where Intel derived only about 15 percent of its revenue. Conversely, Intel received almost 30 percent of its MPU revenue from chips that sold for \$200 or more, a segment in which AMD had no product offerings at all.

This evidence indicates that Intel has enhanced its position in the MPU market since 2006. With less competition from AMD, Intel has greater scope to manage its price structure.¹⁴ Price discrimination stemming from this market power could reduce the information content of

¹⁴ For models of pricing and innovation behavior in the MPU industry, see Aizcorbe and Kortum (2005), Nosko (2010), and Pillai (2013).

its posted list prices, potentially biasing the quality-adjusted indexes generated from these prices. The next section investigates the properties of matched-model and hedonic indexes in the post-2006 pricing environment.

3. MPU Prices: Matched-Model or Hedonic?

As noted, the changes in the pattern of Intel’s posted prices for MPUs raise important questions for price measurement. In this section, we argue that these changes could cause significant biases in a matched-model index (like the PPI) and that hedonic indexes are preferred. We also argue that, given the current pricing environment, the preferred hedonic index relies only on prices in the period of a model’s introduction.

To fix ideas, we briefly describe the matched-model and hedonic price indexes we consider.¹⁵ We then assess how matched-model and hedonic indexes would perform in different pricing environments for MPUs.

Matched-model indexes control for quality change between two periods, say period 0 and period 1, by averaging price changes for models that were in the market in both periods. The underlying idea is to measure “pure” (or quality-adjusted) price change for products whose quality did not change because they were in the market in both periods 0 and 1. However, entry of new products with quality that is different from incumbent products can, in some circumstances, cause bias in matched-model indexes.

For example, consider the case of a new, higher-quality MPU entering the market in period 1 at the same price as an old product sold for in period 0. Because quality has improved, this new MPU represents a drop in quality-adjusted prices. However, matched-model indexes can face challenges in capturing this decline in quality-adjusted prices because the new model

¹⁵ See Aizcorbe (2013) for a recent description of matched-model and hedonic methodology.

does not have an identical model from period 0 with which to compare its prices. For a matched-model index to capture the change in quality-adjusted prices between periods 0 and 1, the price of the old product would need to fall enough in period 1 so that the price *per unit of quality* was equalized across the models. If this equilibration occurs, then the drop in the price of the old model will capture the quality-adjusted price decline implicit in the new, higher-quality model. If the price of the old product does not fall enough in period 1 to equilibrate price per unit of quality (or if the old product is no longer available in the market in period 1), then a matched model index will understate the amount of price decline on a quality-adjusted basis. In the extreme case, where the price of the old product did not fall in period 1 (even while a new higher-quality product was available in the market at the same price), a matched-model index would indicate that quality-adjusted prices were unchanged between the two periods.

Hedonic price indexes identify “pure” price change by explicitly controlling for quality change with measures of product characteristics or performance. A hedonic regression is estimated in which prices are regressed on measures of characteristics or performance and the price change that is left after controlling for quality is identified as quality-adjusted price change. Many alternative specifications have been proposed for hedonic regressions. Perhaps the simplest is to include time dummy variables (time fixed effects) in the hedonic regression and to read off quality-adjusted price change from the coefficients on the time dummies. (We discuss in section 5 our preferred specification for the new price indexes in this paper.)

An issue for hedonic indexes is whether to estimate the regression on all prices or just on prices of products in their period of introduction. Such an introduction-period approach was used in the 1980s for constructing hedonic price indexes for mainframe computers at a time when there was concern that IBM list prices for older models might not be actual transaction

prices.¹⁶ Given similar concerns about prices of older models of Intel MPUs, we also consider introduction-period hedonic indexes.

How well would these alternatives (matched model, full-sample hedonic, and introduction-period hedonic) measure trends in quality-adjusted prices under different explanations for the shift in the pattern of Intel’s posted prices after 2006? These alternative scenarios are highlighted in figure 8, using highly stylized representations of pricing patterns. In these figures, each model is in the market for three periods, and we assume that each successive model is of higher quality than the prior model. Our assessment of the performance of different price indexes under each of these scenarios is summarized in table 3.

We start with the pricing pattern before 2003 (figure 8, panel A). In this scenario, where prices fall as a model ages, all three price index alternatives could capture changes in quality-adjusted prices. For the matched-model index, we need to assume that markets are in equilibrium such that price per unit of quality is at least roughly equalized across models. In that case, the gap between model prices in periods when two models are in the market would represent the value of improved quality, and a matched-model index would correctly adjust for this quality change. For the hedonic indexes, both the full-sample and introduction-period indexes should adequately capture quality change provided that an appropriate measure of quality is available to include on the right-hand side of the hedonic equation. This favorable assessment of all three indexes is designated in table 3 by the “Yes” entries in the first row.

Now, consider the post-2006 pattern of posted prices. As shown in panels B and C of figure 8, new models enter the market at the same list price that exiting models leave the market. We consider two possible scenarios. Panel B illustrates the “age-related discounts” scenario in which transactions prices reflect an increasing discount from posted prices as models age. In

¹⁶ See Dulberger (1986).

Panel B, the solid lines of each color show posted prices for a series of three MPU models, highlighting that posted prices remained flat following a model's introduction. The dashed lines show actual transactions prices. These lines slope downward, as progressively larger discounts are offered on older models as newer, higher performance models become available. In this scenario, a matched-model index would do fine if actual transactions prices (the dashed lines in the figure) were observable. But, a matched-model index based on the *posted* prices would go astray because it would not capture the improvement in quality in successive models. Thus, in the age-related discounts scenario, a matched model index would not capture trends in quality-adjusted prices if the actual transactions prices were unobservable. And, because we only have posted prices for Intel MPUs (see the discussion in section 4), we enter a “no” for matched-model indexes under this scenario in table 3.

In the age-related discounting scenario, a full-sample hedonic index based on observable *posted* prices also would go astray because the posted prices are measured with error. Actual transaction prices of each model are falling over time but a full-sample hedonic index would not account for this measurement error. Accordingly, estimates of quality-adjusted price change from a full-sample hedonic index likely would be biased.

In contrast, the introduction-period hedonic index could correctly capture trends in quality-adjusted prices if the age-related discounts story were operative as in the simple scenario shown in panel B.¹⁷ In particular, the introduction-period hedonic would omit observations in which prices were measured with error, and the performance variables in the regression would control for improvements in quality in successive periods. Thus, we enter a “yes” into the introduction-period hedonic column of the table for this scenario.

¹⁷ Of course, more complex scenarios for time-varying discounts could lead to biases in an introduction-period hedonic index. This would happen, for example, if the list price and transaction price do not coincide at the time of introduction and the difference across those prices varies over time or across models.

Panel C of figure 8 highlights another scenario (“Dropoff in volume”) that could create challenges for accurately measuring quality-adjusted price changes. In this scenario, posted prices do not change, but the quantity purchased of a specific model drops off as the model gets older and faces competition from newer, more powerful models with lower prices per unit of quality. In panel C, the solid, heavier line represents the early, high-quantity part of each model’s life cycle and the thinner line represents the later part when sales have dropped. If model-level data on shipments or sales were available, a shipments- or sales-weighted index would account for the declining importance of the older model. However, we do not have model-level quantity data. Accordingly, we are forced to consider price indexes that put equal weight on every observation.

Under our assumption that quality is improving over time, an unweighted matched-model and an unweighted full-sample hedonic index would be problematic as they would put too much weight on price observations for which there were few transactions. In contrast, in this scenario an introduction-period hedonic seems more likely to capture the trend in quality-adjusted prices than would an unweighted matched-model index or a full-sample hedonic index. By focusing on prices at the beginning of each model’s life-cycle, a regression that applies equal weights to all observations avoids over-weighting models whose quantities have dropped off. Thus, in the final row of the table, we enter a “no” for a matched-model and full-sample hedonic index and a “yes” for the introduction-period hedonic.

The assessments in table 3 indicate that, under a range of scenarios associated with the shift in Intel’s pricing behavior, an introduction-period hedonic index is preferred. Accordingly, we focus on these indexes, though we also report matched-model indexes and hedonic indexes based on full-sample estimates.

4. Data

Our MPU prices are collected from publicly available Intel price lists for the period from 1999 to 2013.¹⁸ Intel announces wholesale list prices several times a year for MPUs sold in multiples of 1,000. Unlike single units sold in retail channels, these “trays” of MPUs do not include a cooling system and carry a shorter warranty. Models are identified by family (for example, Core i7, Pentium, Core 2 Duo), model ID (for example, i7-4960X), and selected technical characteristics (for example, amount of cache memory or clock speed). We merged these price lists to create price data at a quarterly frequency. We restrict our attention to the 255 MPU models for desktop computer systems introduced between 2000 and 2012.¹⁹ As shown on line 1 in table 4, 101 of these models are observed in the 2000-2006 period and 166 in the 2006-2012 period; these two counts sum to more than 255 because some chips introduced in 2006 are included in both sub-period counts. In addition, the average model has prices observed for 6 quarters so we have many more quarterly price observations than models. At the time of introduction, the average price per MPU model was \$495 during 2000-2006 and \$284 during 2006-2012 (line 3 of the table).

Information on the relative quality of the chips came from test results for specific representative tasks, or “benchmarks,” provided by the System Performance Evaluation Corporation (SPEC), a non-profit corporation that publishes these measures as a service to the technology industry and user communities. Benchmark test results are available for individual tasks that rely heavily on integer computation (such as word processing) and for tasks that rely

¹⁸ Price lists for the period from April 1999 to December 2006 were collected from an archived version of a website devoted to computer hardware. Price lists for later dates were taken directly from Intel’s website. On dates when both sources were available, we confirmed that the website prices matched Intel price lists.

¹⁹ We exclude models marketed to the low-performance segment, for which the SPEC benchmarks may not be a suitable measure of performance as valued by the system user.

heavily on floating point computation (such as speech recognition). Scores for individual tasks are measured in seconds, although SPEC rescales these scores so that higher scores indicate better performance and the units are no longer in seconds. SPEC provides an overall score both for integer and for floating-point computation, which is calculated as a geometric mean of scores for the specific tasks related to each type of computation. For our preferred single measure of performance, we take the geometric mean of the overall scores for integer and floating-point tasks.²⁰

SPEC benchmarks provide several ways to measure MPU performance. The performance of a single task is measured by the “speed” score and the performance of multiple tasks is measured by the “rate” score. The “speed” and “rate” scores differ in their use of parallel processing, an important consideration after the introduction of multi-core MPUs in the mid-2000s. In the “speed” test, a single task may be broken into component calculations to be run on different processing cores on the MPU. In the “rate” test, multiple instances of the same task may be run simultaneously to more fully exploit the potential of the chip. We use the “speed” score as our base case, but we also report results using the “rate” score in the appendix.²¹

An MPU chip often has multiple scores for each of the SPEC benchmark tests. Multiple scores can arise either because more than one computer vendor tested the chip or because a given vendor tested the chip under different conditions. The variation in test conditions can reflect differences in hardware (e.g., the circuit board or amount and type of DRAM) or software (e.g.,

²⁰ Specifically, we used results for the CPU2000 and CPU2006 benchmark suites. The composite scores for integer tasks and floating-point tasks are highly correlated.

²¹ For both “speed” and “rate” tests, scores are available for “base” test runs, which restrict the tester’s tuning of the compilation of the source code, and for “peak” runs, which allow testers to tune the compiler more aggressively. For our analysis, we report scores for the “base” test runs; peak” scores yield similar results, as shown in the appendix.

the operating system or compiler). When multiple scores are available for a specific model, we use the model's median score.²²

We matched 157 MPU models from our price data to at least one performance score published by SPEC. Some of these are 2006 models that are evaluated on both the 2000 and 2006 vintage test suites. Allowing for the fact that these models are counted twice, line 2 of table 4 indicates that our dataset includes 78 models for the period 2000-2006 and 90 models for the period 2006-2012).

Average performance scores are shown on line 4 of the table. SPEC changed the scaling of these scores in the new benchmarks introduced in 2006 so the scores during the 2000-06 period are not directly comparable to those from the 2006-12 period. As noted, however, both benchmark suites were used to test for chips in 2006 so we are able to splice across the two periods.

We supplemented the matched price and performance data with information collected on thermal design power (TDP), which measures the amount of heat generated when running typical software for the chip. The amount of heat generated (measured in watts) is closely related to the MPU's power consumption. This information is collected from Intel's product information database (<http://ark.intel.com>). Average thermal design power for chips in our sample is reported on line 5 of the table.

²² As discussed in the appendix, we also estimated specifications that included each model-score pair as an observation (rather than considering each model to be an observation). For example, if three scores were reported for a model, we included three observations for that model with each different score. In these specifications, we included controls for the company doing the testing and the amount of system memory.

5. Specification of the Hedonic Regressions

To fix ideas, we first describe a dummy-variable hedonic specification:

$$\ln(P_{i,t}) = \alpha + \sum_k \beta_k \ln(X_{k,i,t}) + \sum_t \delta_t D_{i,t} + \varepsilon_{i,t} \quad (1)$$

where $P_{i,t}$ is the price of chip i in period t , $X_{k,i,t}$ is the value of characteristic k for chip i in period t , $D_{i,t \in Y}$ is a vector of time dummy variables (fixed effects) that equals 1 if chip i is observed in quarter t and zero otherwise, and $\varepsilon_{i,t}$ is an error term.

One potential shortcoming of equation 1, highlighted by Pakes (2003) and Erickson and Pakes (2011), is that the coefficients on the characteristic or performance variables are constrained to remain constant over the full sample period. One response to that concern is to run a cross-section regression for every time period and then to use results from those regressions to build up a price index.²³ Such an approach is appealing because it provides maximum flexibility for estimated coefficients to change over time and it provides the flexibility to use price index formulas. However, our sample size is too small to run reliable cross-section hedonic regressions for every quarter or even every year.

As a compromise, we focus on adjacent-period (in our case, adjacent year) hedonic regressions.²⁴ Specifically, we estimate for each two-year overlapping period the following regression:

$$\ln(P_{i,t}) = \alpha + \sum_k \beta_k \ln(X_{k,i,t}) + \delta D_2 + \varepsilon_{i,t} \quad (2)$$

where $P_{i,t}$ is the price of chip i in year t . We measure $P_{i,t}$ as the average of the observed prices within the year.²⁵ The dummy variable D_2 equals 1 if the price observation is in the second year of the two-year overlapping period and 0 otherwise. To construct a price index from this

²³ See Aizcorbe's (2013) discussion and the references there.

²⁴ See Triplett (2006) for a discussion of adjacent-period hedonic regressions.

²⁵ We also estimated regressions at the quarterly frequency for each two-year period and included a time trend spanning the eight quarters of data included in each regression. That alternative yielded price trends similar to those reported here.

sequence of regressions, we spliced together the percent changes implied by the estimated coefficients on the D_2 variables. As noted above, we rely on the SPEC variable to capture the performance of each MPU. We believe that this variable provides a comprehensive gauge of each MPUs performance, as experienced by users. We also include thermal design power (TDP) to capture the amount of heat generated by each MPU. If greater heat generation and the associated power use is viewed as undesirable by users, this variable might be expected to have a negative coefficient. On the other hand, this variable could pick up elements of performance not captured in the SPEC benchmarks, in which case the sign of the coefficient could be negative or positive.

As noted in the previous section, SPEC updated its suite of performance tests in 2006. . We use the older (SPEC 2000) benchmarks for the adjacent-year regressions through 2005-2006 and the newer (SPEC 2006) benchmarks for the adjacent-year regressions beginning with 2006-2007.

6. Results

Table 5 shows estimates of the hedonic regression in equation 2 for the overlapping two-year periods during 2000-2006, and table 6 shows estimates for 2006-2012. The upper panel in each table presents estimates that rely only on prices in each MPU model's introduction period, while the lower panel presents estimates based on the full sample of price observations. The coefficients on the time dummy variable in each two-year overlapping period provide an estimate of the average annual rate of change in quality-adjusted MPU prices within that period. As noted, the variables *Performance* (based on the performance benchmark scores from SPEC) and *Power* (thermal design power) capture elements of the quality of each model.

Overall, the variables span much of the variation in MPU prices. The adjusted R^2 averages close to 0.60 across the full set of regressions shown in tables 5 and 6.

Although Pakes (2003) cautions against providing structural interpretations of the coefficients, we note that the coefficients on *Performance* are uniformly positive and are significant at the 5 percent level in about three-quarters of the regressions. These coefficients indicate that higher performing MPU models sell for higher prices and suggest that *Performance* is capturing an important element of quality differences across MPU models. The coefficients on the *Power* variable are positive and significant in the majority of the regressions. This result suggests that heat generation may not be a major issue for desktop PCs and that, perhaps, MPUs generating more heat perform at higher levels (and therefore sell for higher prices) in ways not captured by *Performance*. In contrast, for laptops, where heat dissipation likely is a more challenging problem than for desktops, Sun (2014) finds that estimated coefficients on power generally are negative.

To construct annual price indexes from these regressions, we set the 2000 value of the index to 100, and then use the implied change over subsequent years from each overlapping period regression. For example, to calculate the annual rate of change from 2000 to 2001, we exponentiate the coefficient on the dummy variable for 2001 observations.²⁶

We summarize our results in table 7 and figure 9. The table reports average rates of price change over 2000-2008 and 2008-2012 from five different measures: a hedonic index for the full sample, an introduction-period only sample (our preferred index), the PPI, a “PPI-like” matched model index calculated on our sample of Intel prices for desktop MPUs, and an index of

²⁶ Because the exponential function is nonlinear, the translation from log prices to price levels requires a term in the variance of the residual to be strictly unbiased. We will incorporate this adjustment in the next draft of the paper. Preliminary work suggests that this adjustment will not affect our basic story.

semiconductor prices prepared by the Federal Reserve Board.²⁷ We divide the 2000-2012 period at 2008 because that is the point at which our preferred hedonic index and the PPI begin to differ. The figure plots the levels of the PPI and both hedonic indexes.

From 2000 to 2008, all of the indexes show very rapid declines in MPU prices. As discussed in section 3, with Intel's ubiquitous downward re-pricing of existing chips before the mid-2000s, all of the price indexes—both matched model and hedonic—would be expected to capture the downward trend in quality-adjusted prices. This expectation is borne out by our results. As shown in table 7, all of the price indexes for MPUs show average annual declines of 33 percent or more over 2000-08. In addition, there is no difference between the rate of decline of our preferred entry-price hedonic index and the PPI — both drop an average of 39 percent annually over this period.

However, the trends in the indexes diverge after 2008. Strikingly, the introduction-period hedonic continued to decline as rapidly as before 2008, while the decline in the PPI slowed sharply. Indeed, the PPI fell at an average annual rate of only 9 percent from 2008 to 2012 and was barely falling by 2012. For the reasons highlighted earlier in the paper, we believe that these results point to likely bias in the PPI for MPUs. The lack of any slowdown in the preferred hedonic index suggests that the PPI could be providing a deeply misleading picture of price trends for MPUs in recent years.

One possible concern about this argument is that our sample of prices or coverage of models could differ in a consequential way from that used for the PPI. To demonstrate that coverage and sample likely are not the source of the faster price decline that we observe with hedonic price indexes, we calculated a matched-model index using the same Intel price data for

²⁷ The Federal Reserve index is a matched-model index from 1992 to 2006 and an introduction-period only hedonic index after 2006. It parallels an early version of the analysis described in this paper, but the dataset and regression specification differ somewhat from the indexes presented here.

desktop MPUs that we used to estimate the hedonic regressions. These estimates are shown in table 7 in the line labeled “PPI-like” matched model. We use this label because the matched-model calculation roughly follows the PPI procedure, while our sample and coverage differ from the PPI. The trends in this index nearly match those in the PPI, suggesting that the key difference between our preferred index and the PPI is not due to sample or coverage.

Although the decline in the full-sample hedonic index did not slow after 2008 to nearly the same extent as the PPI, it did drop off somewhat relative to the introduction-period index. As indicated by the analysis in section 3, this pattern is what would be expected under the “age-related discounting” and “drop-off in volume” scenarios if Intel were keeping posted prices for older model fixed to a greater degree than previously. Because discounts from posted prices on older models are unobservable, the full-sample index will understate price declines — and by a larger amount than when posted prices were more flexible. Moreover, to the extent that Intel is allowing quality-adjusted prices on older models to rise above those for new models, sales of the older models likely is falling off more substantially than when posted prices fell over a chip's life cycle. Given that we do not have model-level shipments data, the index based on the unweighted full-sample index will overweight the older models whose prices are not changing. Under either scenario (or a combination of them), the full-sample hedonic index will understate the rate of price decline, supporting our preference for the introduction-period index.

7. Conclusion

After falling rapidly through the mid-2000s, the PPI for MPUs has declined very slowly by historical standards in recent years. Such a slowdown is puzzling given evidence of ongoing rapid advances in semiconductor technology. To reconcile these observations, this paper

demonstrates that the matched-model procedure used for the PPI for MPUs likely is inappropriate in the pricing regime that Intel — the dominant manufacturer — adopted in the mid-2000s. We argue that a hedonic approach based on introduction-period prices is the preferred way to measure quality-adjusted MPU prices in the current pricing environment. Results from such a hedonic price index indicate that quality-adjusted MPU prices continued to fall rapidly after the mid-2000s. Indeed, our figures show an average annual decline of 39 percent in MPU prices over 2008-2012, compared with only 9 percent in the PPI (and barely any decline by 2012). This discrepancy has important implications for understanding the rate of technical progress in the semiconductor sector and, arguably, for the broader debate about the pace of innovation in the U.S. economy.

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Table 1. Semiconductor Technology Cycles
 (Years needed for 30 percent reduction in linear scaling)

Industry Frontier			Intel MPU Chips	
Period	Years		Period	Years
1969-1993	3.0		1971-1994	2.9
1993-2012	2.1		1994-2012	1.9
1993-2003	1.9		1994-2004	1.9
2003-2012	2.3		2004-2012	2.0

Source: Byrne, Oliner, and Sichel (2013).

Table 2. Performance of Entering versus Incumbent MPUs

(All statistics refer to mid-range and high-end Intel desktop MPU chips)

	2000-03	2004-06	2006-09	2010-12
Share of entering chips with performance scores above highest incumbent performance score (pct.)	68.4	25.8	43.1	32.3
Ratio of average entrant performance score to highest incumbent performance score	1.046	.965	.950	.889

Source. Authors' calculations based on data from System Performance Evaluation Corporation. Authors' composite performance score is a geometric mean of scores from integer and floating point benchmark tests from SPEC CPU2000 and SPEC CPU2006.

Table 3. Implications of Alternative Scenarios for Matched-Model and Hedonic Price Indexes

		Will index capture trend in quality-adjusted prices?		
	Panel in Fig. 8	Matched model	Full-sample hedonic	Introduction-period hedonic
Pre-2003 pattern	A	Yes	Yes	Yes
Post-2006 pattern				
Age-related discounting	B	No	No	Yes
Drop-off in volume	C	No	No	Yes

Table 4. Summary Statistics

(All statistics refer to mid-range and high-end Intel desktop MPU chips)

Panel A				
	2000-06		2006-12	
	Number of models	Quarterly price obs.	Number of models	Quarterly price obs.
1. Chips on Intel price lists	101	651	166	1047
2. matched to SPEC scores	78	416	90	605
Panel B				
	2000-06		2006-12	
Chip characteristics, average (standard deviation in parentheses)	Introduction period	Over lifecycle	Introduction period	Over lifecycle
3. MPU price (\$)	495 (267)	321 (247)	284 (276)	252 (242)
4. SPEC performance score ¹	1282.0 (650.5)	1392.0 (674.1)	28.2 (12.4)	26.6 (12.0)
5. Thermal design power (watts)	77.0 (28.2)	77.1 (30.2)	82.6 (27.5)	81.2 (25.1)

1. Score for each MPU chip is the median across test results, which differ with respect to testing vendor and system characteristics (for example, amount of DRAM, operating system) with individual performance scores calculated as the geometric mean of overall floating point and overall integer benchmark tests from SPEC CPU2000 and SPEC CPU2006.

Source. Authors' calculations based on data from System Performance Evaluation Corporation, Intel price lists, and data from <http://ark.intel.com>.

Table 5. Regression Results for 2000-06

Panel A: Introduction period only

	2000-01	2001-02	2002-03	2003-04	2004-05	2005-06
<i>Time trend</i>	-.824** (.190)	-.177 (.233)	-1.029** (.342)	-.550 (.356)	-.118 (.136)	-.620** (.199)
<i>ln Performance</i>	.97 (.57)	.38 (.51)	1.56 (1.67)	3.06 (1.87)	2.99** (.67)	3.00** (.49)
<i>ln Power</i>	-.33 (.41)	.73 (.44)	.78 (1.33)	.26 (1.53)	2.11** (.38)	1.50** (.27)
Number of Obs.	19	17	18	16	22	26
Adjusted R ²	.50	.47	.31	.39	.83	.73

Panel B: Full sample

	2000-01	2001-02	2002-03	2003-04	2004-05	2005-06
<i>Time trend</i>	-.818** (.078)	-.417** (.073)	-.495** (.148)	-.324* (.137)	-.131 (.120)	-.299** (.105)
<i>ln Performance</i>	1.36** (.22)	1.27** (.19)	1.34** (.34)	.77 (.80)	.80 (.44)	1.86** (.27)
<i>ln Power</i>	-.27 (.16)	-.31 (.16)	-.28 (.34)	1.38 (.79)	2.14** (.42)	1.53** (.24)
Number of Obs.	36	45	42	37	49	60
Adjusted R ²	.81	.72	.52	.52	.63	.63

Note: The dependent variable is ln(MPU price); the regression includes a constant, not shown above. Standard errors are in parentheses. * and ** indicate significance at the 5% and 1% levels, respectively.

Table 6. Regression Results for 2006-12

Panel A: Introduction period only

	2006-07	2007-08	2008-09	2009-10	2010-11	2011-12
<i>Time trend</i>	-.459 (.239)	-.239 (.226)	-.824* (.360)	-.417 (.249)	-.568* (.226)	-.198 (.161)
<i>ln Performance</i>	1.58** (.47)	1.61* (.58)	2.37** (.76)	2.04* (.81)	1.28 (.62)	1.49* (.58)
<i>ln Power</i>	1.84** (.30)	1.49** (.28)	.77* (.30)	.73 (.46)	1.20** (.27)	.90** (.22)
Number of Obs.	24	27	27	22	21	25
Adjusted R ²	.69	.66	.52	.46	.74	.66

Panel B: Full sample

	2006-07	2007-08	2008-09	2009-10	2010-11	2011-12
<i>Time trend</i>	-.467* (.175)	-.254* (.119)	-.460** (.122)	-.170 (.100)	-.299** (.105)	-.341** (.122)
<i>ln Performance</i>	1.89** (.32)	1.81** (.26)	1.43** (.20)	1.28** (.15)	.81** (.15)	.57** (.17)
<i>ln Power</i>	1.50** (.23)	1.48** (.17)	1.00** (.16)	.68** (.16)	.95** (.17)	1.02** (.16)
Number of Obs.	35	53	66	70	76	62
Adjusted R ²	.70	.72	.62	.60	.47	.50

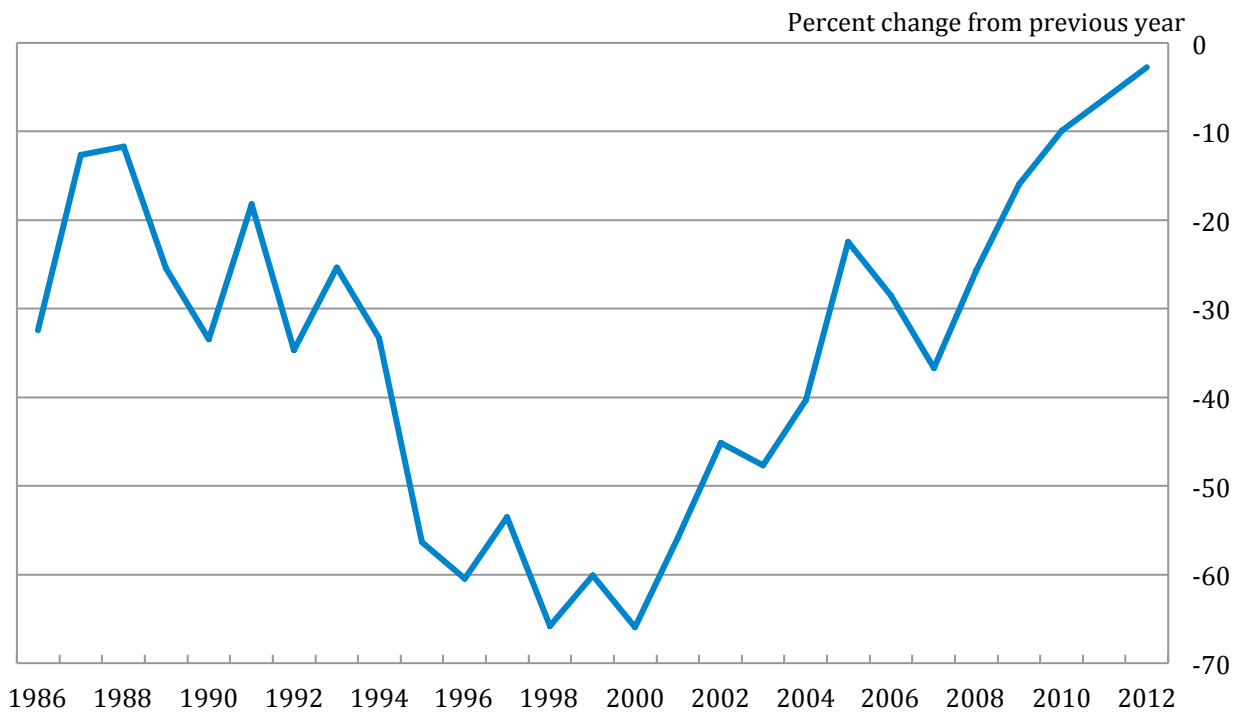
Note: The dependent variable is ln(MPU price); the regression includes a constant, not shown above. Standard errors are in parentheses. * and ** indicate significance at the 5% and 1% levels, respectively.

Table 7. Rates of change in MPU prices
(Average annual percent change over periods shown)

	2000-08	2008-12
Hedonic, adjacent periods		
Full sample	-33	-27
Introduction-period	-39	-39
PPI	-39	-9
"PPI-like" matched model, desktop MPUs	-44	-12
FRB ¹	-40	-31

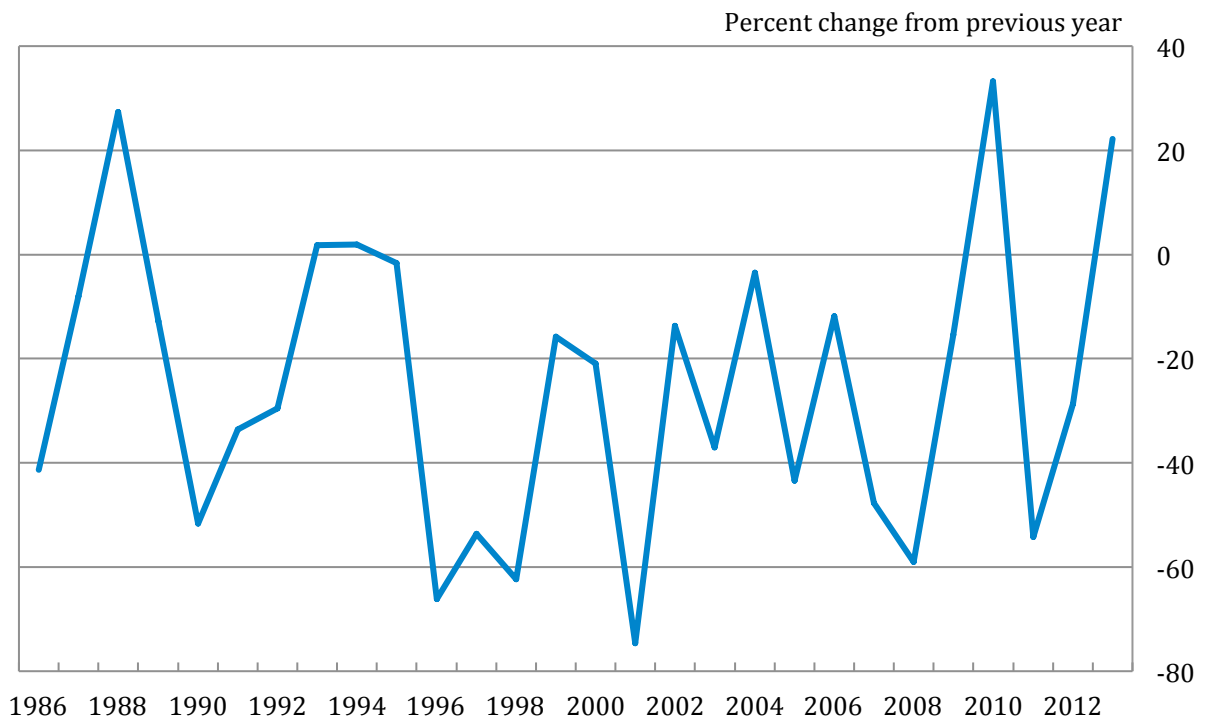
1. Constructed as a matched-model index through 2006 and as an introduction-period hedonic index after 2006. The dataset and regression specification differ somewhat from the introduction-period hedonic regression estimated in this paper.

Figure 1: MPU Prices



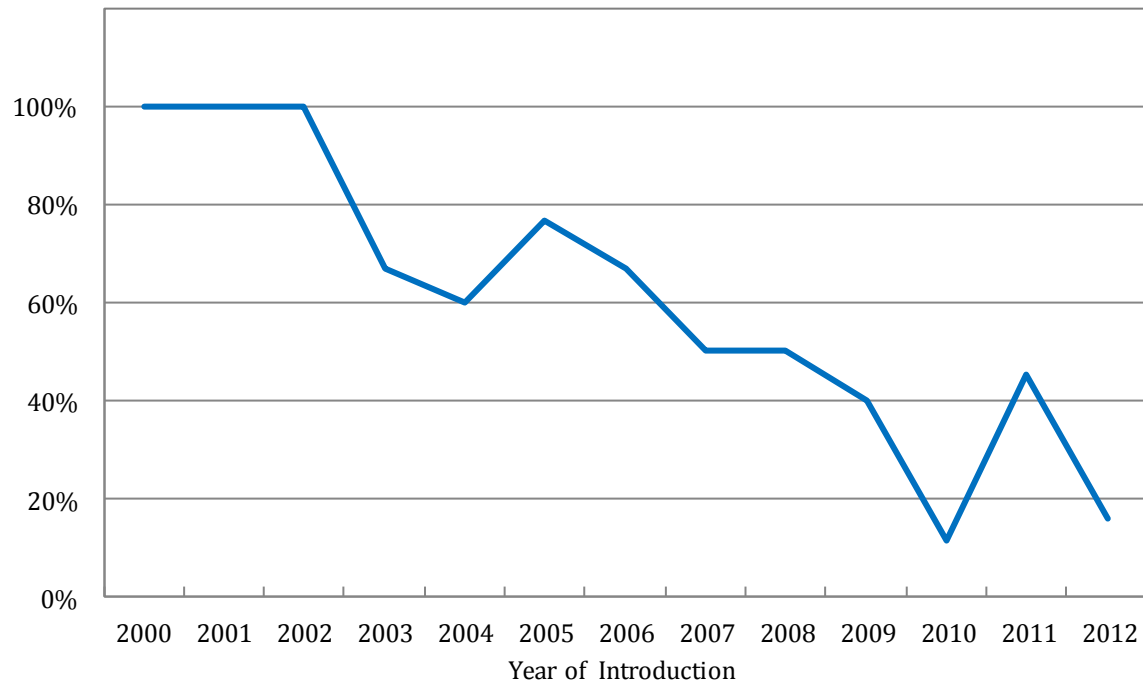
Sources. Grimm (1998, table 12) for 1986-92, Federal Reserve Board for 1993-97, and Bureau of Labor Statistics for 1998-2012.

Figure 2: DRAM Prices



Sources. Grimm (1988, table 5) for 1986-92 and Federal Reserve Board for 1993-2013.

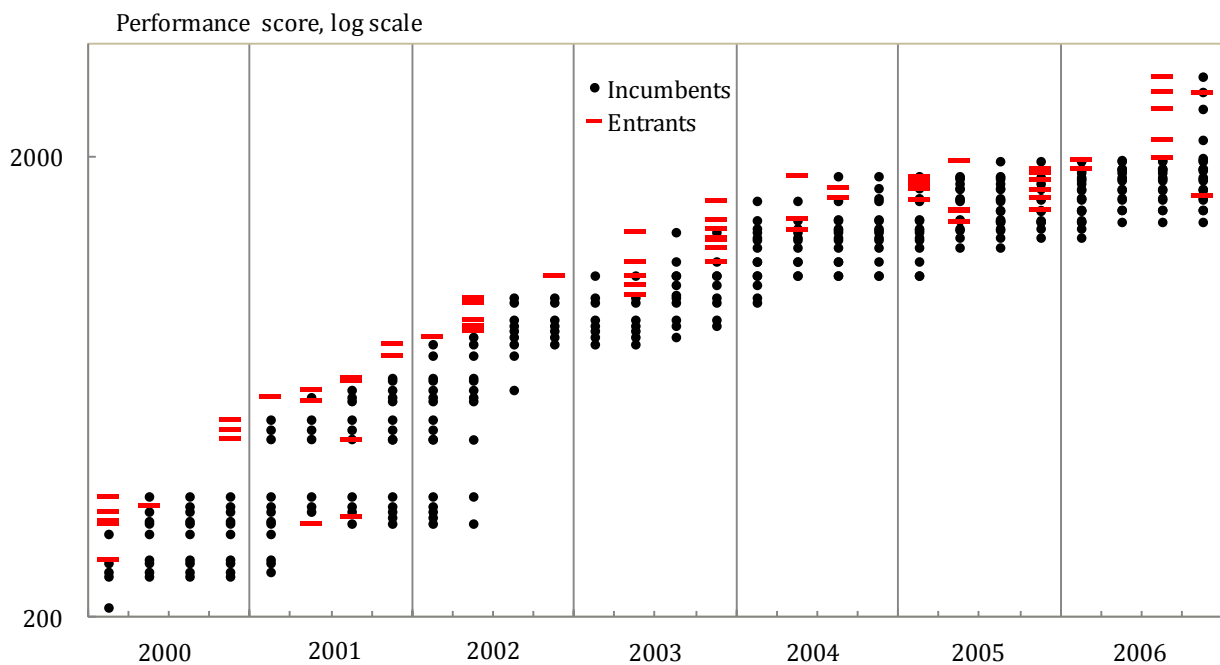
Figure 3: Share of Intel MPUs with List Price Decline within Four Quarters of Introduction



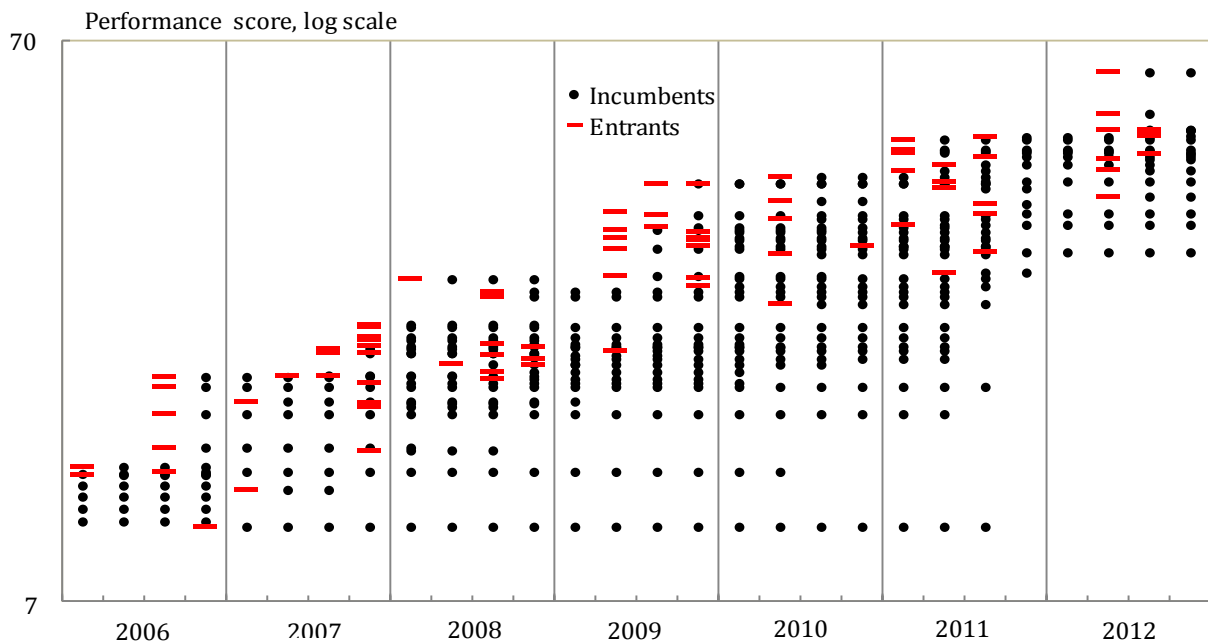
Source. Authors' calculations from Intel price lists.

Figure 4: Performance of Entering and Incumbent Intel Desktop MPUs

Panel A: 2000-06



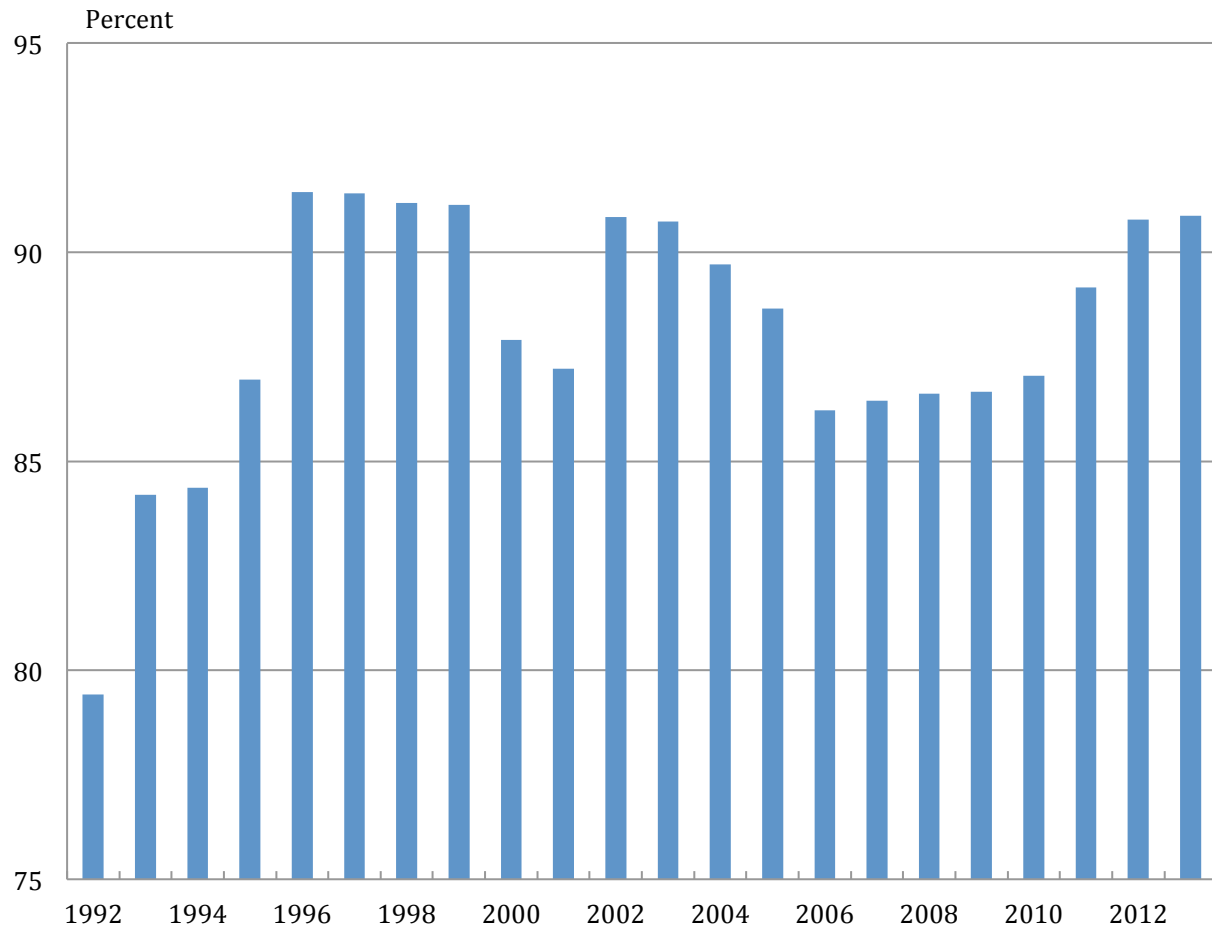
Panel B: 2006-12



Note. Authors' performance score is a geometric mean of scores from integer and floating point benchmark tests from SPEC CPU2000 and SPEC CPU2006. The performance score for each model is the median score provided for each MPU. The scale for the 2000-06 period differs from the scale for the 2006-12 period.

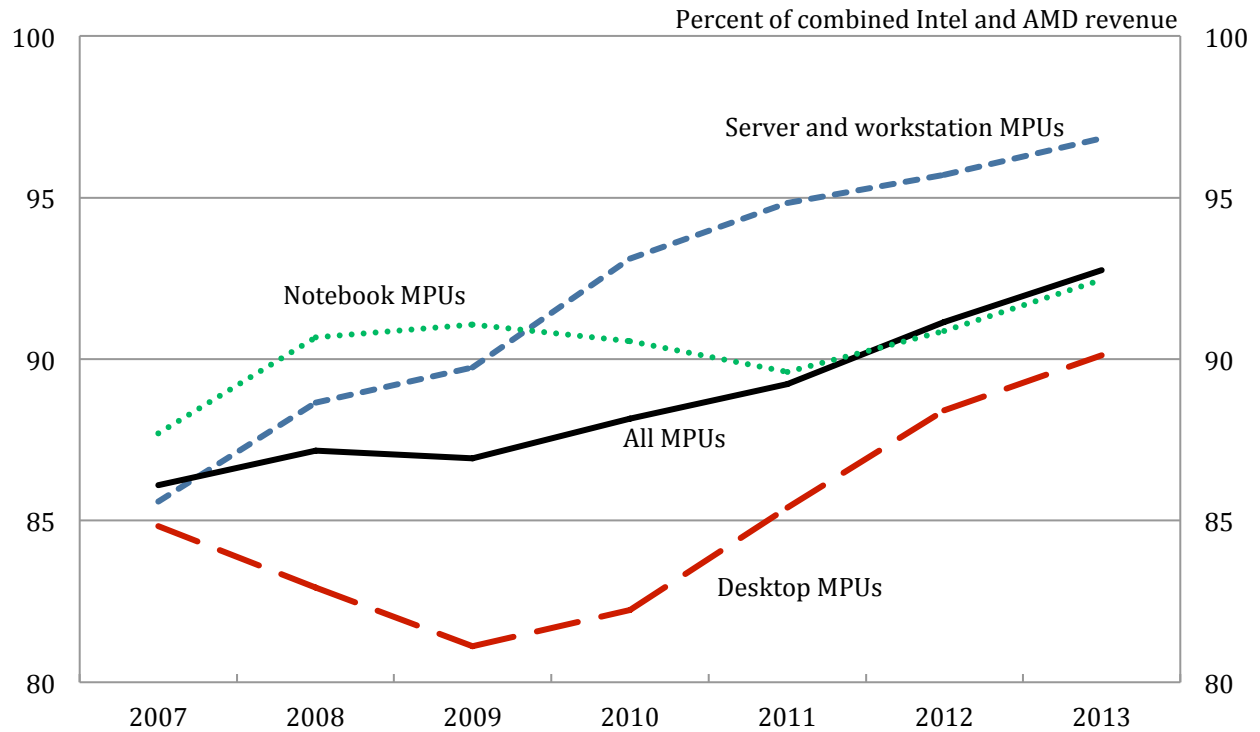
Source. Authors' calculations based on data from System Performance Evaluation Corporation.

Figure 5: Intel Share of Combined Intel and AMD Revenue



Source. Authors' calculations based on data from financial reports filed with the Securities and Exchange Commission.

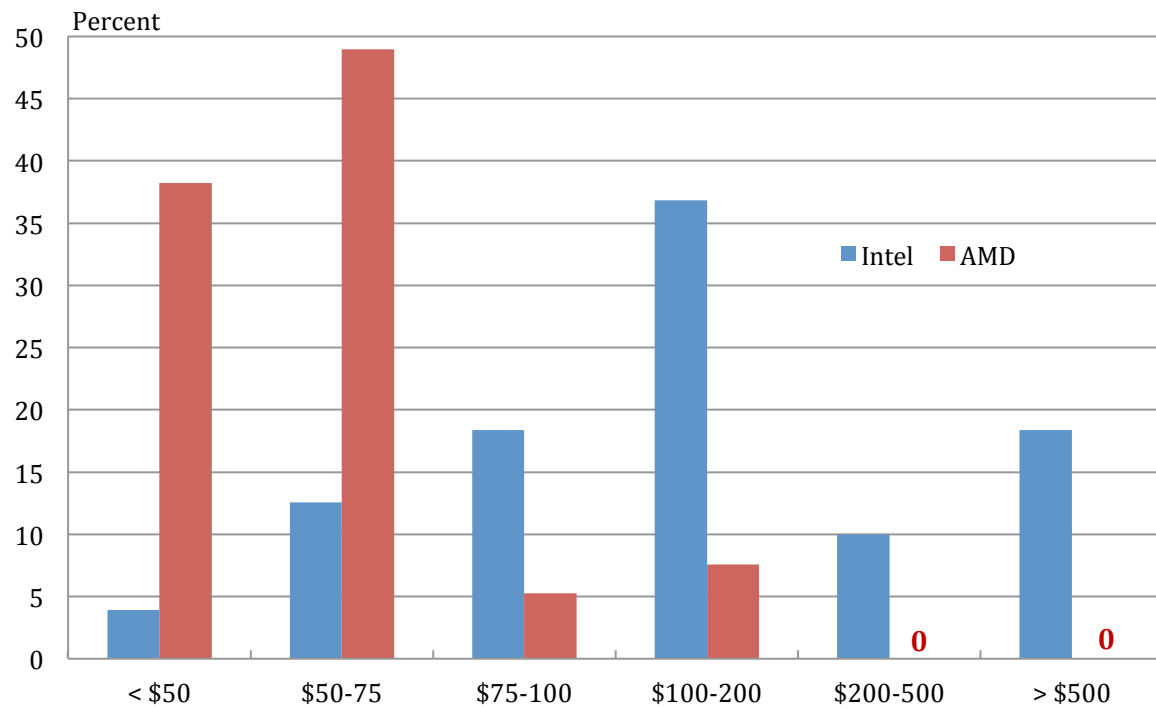
Figure 6: Intel Market Shares, MPUs



Note. Data for 2013 cover Q1 through Q3.

Source. Authors' calculations based on data from IDC Research, Inc.

Figure 7: 2013 Distribution of Desktop MPU Revenue, by Price of Chip

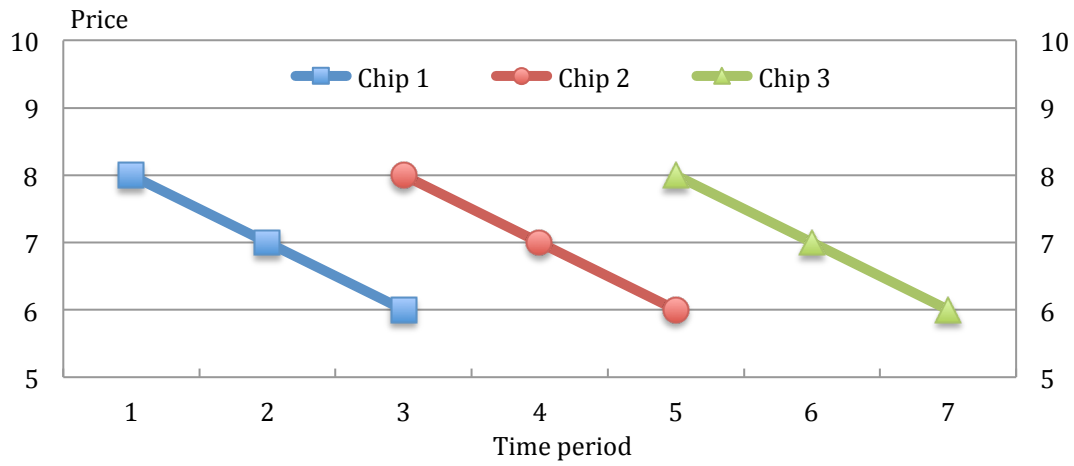


Note. Data cover 2013:Q1 through 2013:Q3.

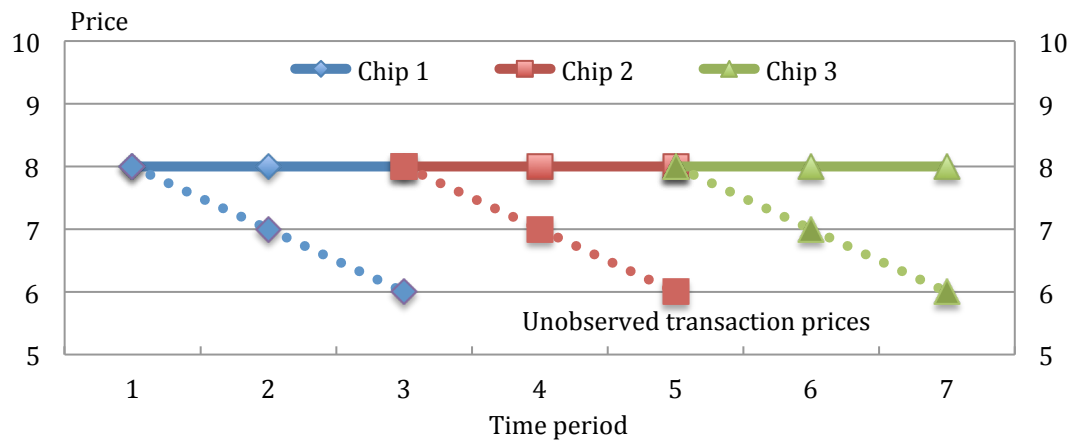
Source. Authors' calculations based on data from IDC Research, Inc.

Figure 8: Alternative Scenarios

Panel A: Pre-2003



Panel B: Post-2006, Age-related Discounts



Panel C: Post-2006, Drop-off in Volume

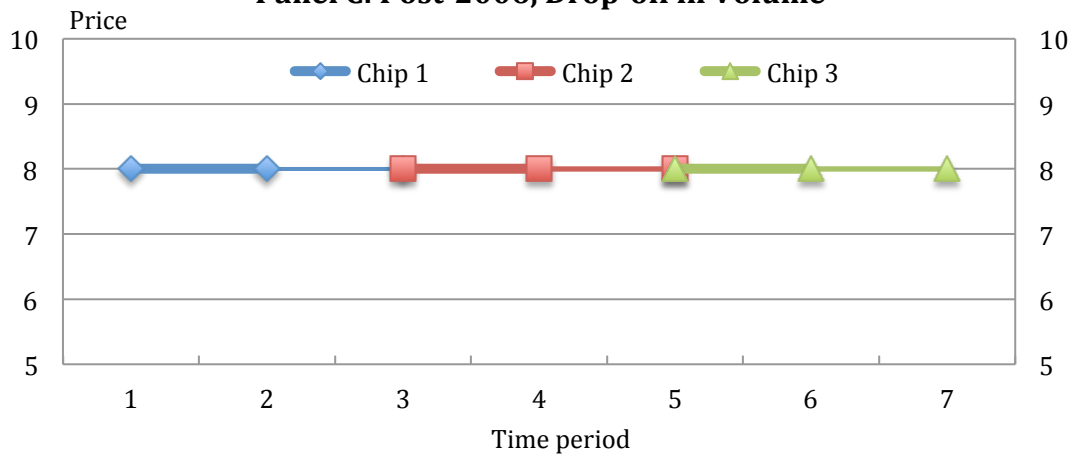
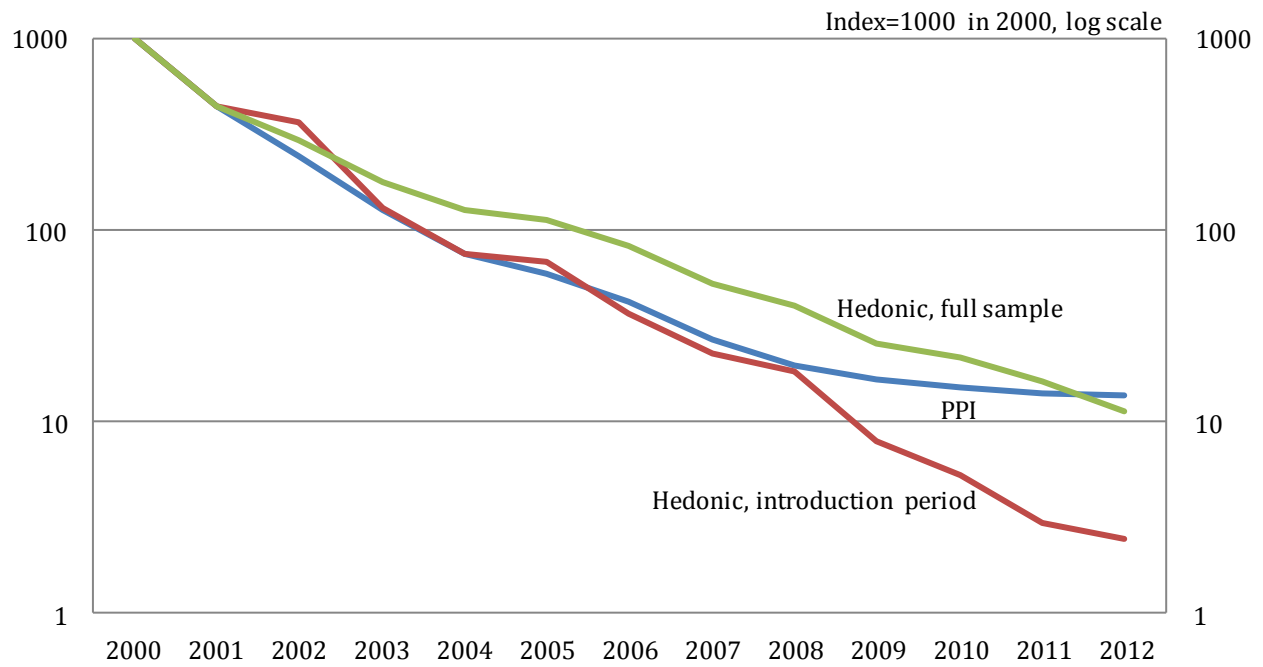


Figure 9: MPU Price Levels



Source. Bureau of Labor Statistics and authors' calculations.

Appendix: Alternate Specifications

Multiple benchmark test scores are available for most microprocessors in our data. In our preferred specification, discussed in the body of the paper, we construct a single measure of performance. We consider several alternate specifications to assess the sensitivity of our results to the method employed to summarize test scores. In all cases, we estimate adjacent-year regressions with introduction-period prices. A comparison of the resulting indexes is shown in Table A.1.

As noted in section 4, SPEC benchmarks provide several ways to measure MPU performance. One dimension along which the benchmarks vary concerns the use of parallel processing. In the “speed” test, a single task may be broken into component calculations to be run on different processing cores on the MPU. In the “rate” test, multiple instances of the same task may be run simultaneously to more fully exploit the potential of chips with multiple cores. We use the “speed” scores in the baseline regression, as sufficient data on “rate” scores are only available beginning in 2006. Results for regressions using the “rate” scores (but otherwise identical to the baseline regression) are shown on line 2 of the table and differ only slightly from the baseline regression results shown on line 1.

The benchmark test results can also differ regarding the extent to which testers adjust the compilation of the computer source code to make optimal use of the test hardware. In the baseline results, SPEC specifies how the source code is compiled (these are called “base” test results). SPEC also collects results produced with fewer constraints, allowing more aggressive “tuning” of the compiler. Results using these “peak” scores are shown on line 3. These are very similar to the baseline results with the exception of the 2003-2006 period when the price index based on peak scores falls noticeably more slowly.

Even when the SPEC scores are limited to those with "base" tuning of the compiler and the "speed" specification for parallel processing, there are multiple scores for some MPU chips. The multiple scores arise from testing by different vendors and the use of differing amounts of system memory (DRAM). In the baseline results reported in the paper, we employ the median test score reported by SPEC for an MPU with the "base" tuning of the compiler and the "speed" specification. Results using the maximum rather than the median score reported for the MPU model are shown on line 4. This hedonic index tracks our baseline index except for the 2009-2012 period, when it falls more slowly.

Both the baseline regression and the alternatives considered above collapse the multiple SPEC scores to a single number. Our final robustness check unpacks the collapsed score and includes a separate observation for each of the reported SPEC scores with the "base" tuning and the "speed" specification. We use dummy variables to control for the vendor reporting the test results and include a variable for the amount of DRAM employed in the test. It is important to note that the price of the MPU does not vary across these observations. The unpacking effectively introduces multiple copies of what had been a single MPU price observation, increasing the weight the regression places on MPUs with more test scores. As shown on line 5 of the table, this regression generates a somewhat slower decline in MPU prices over 2000-09 than the baseline, but leaves the 2009-12 decline about unchanged.

All in all, these variations on the baseline regression do not affect the central conclusion in the paper — that constant-quality MPU prices have continued to decline rapidly, in contrast to the picture from the PPI.

Table A.1 Rates of Change in MPU Prices for Alternate Specifications
(Average annual percent change over periods shown)

	2000-12	2000-03	2003-06	2006-09	2009-12
1. Baseline	-39	-49	-35	-40	-33
2. "Rate" scores	NA	NA	NA	-41	-32
3. "Peak" scores	-38	-49	-28	-41	-32
4. Max. score	-38	-50	-33	-39	-25
5. System controls	-34	-40	-23	-36	-34

1. Results for adjacent-year regressions estimated with entry prices.